FOURTH QUARTERLY REPORT

ON

BONDING LARGE AREA SILICON WAFERS

JET PROPULSION LABORATORY

CALIFORNIA INSTITUTE OF TECHNOLOGY

PASADENA, CALIFORNIA

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CONTRACT NO. 952022

PREPARED FOR

JET PROPULSION LABORATORY

4800 Oak Grove Drive

Pasadena, California 91103

PREPARED BY

MOTOROLA INC.

SEMICONDUCTOR PRODUCTS DIVISION

5005 E. McDowell Road

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ABSTRACT

Progress in both solid-liquid and solid-solid interdiffusion bonding of large area wafers to substrates is described. The liquid bonds are primarily fabricated of Au with In and/or Sn as the "wet" layer. The solid state bonds have been made chiefly with the Au-Ag system. The problem of voiding which dominates both the SLID and SSID bonding projects is discussed as to causes and possible solutions. Bonds of 2-inch multidevice wafers to molybdenum substrates using both methods have been made and the devices tested. Initial data on the thermophysical properties phase of the program are presented. These include the thermoconductivity of several eutectic alloys and alloys of the Ag-In system. Also the thermal expansion of the Ag-In solid solution is presented. Modifications in the mechanical properties measurements along with progress in this phase are also described.

The first data from the stress analysis computer program yields some insight into the stress patterns of a trilayer bond system using gold solder. These results indicate a certain "transparency-to-stress" in the solder layers used to make bonds. Implications on fabrication of new solders and future bonds are discussed.

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1.0 INTRODUCTION

This report describes work performed during the fourth 3-month period of an 18-month program to develop techniques for reliably bonding large area silicon wafers to suitable heat sinks. The purpose is to enable bonding of silicon single crystals greater than 10,000 square mils in area and up to 2 inches in diameter in a manner which does not damage the wafer. In addition, the electrical properties of the semiconductor devices constructed in the wafer must not be altered, while the provision of a low thermal resistance path is a necessity. The system should not degrade under repeated thermal shock or other high stress testing which simulates operation.

Phase one of this program is the study of basic properties of potential bonding materials and the development of techniques suitable to large area application. This phase has matured and the selection of suitable metal systems is near completion. Development of methods for the efficient use of these materials is in progress.

A unique soldering technique--diffusion bonding--has emerged as most attractive for accomplishing the required task. In a variety of forms, each suitable for a specific purpose, this method achieves a high melting point solder bond while employing a low temperature anneal. This enables the use of "brazing" type solders without introducing the excessive strains of a high temperature excursion. Recent accomplishments using all solid state diffusion bonds and the original solid-liquid diffusion bonds are described in section 2.1. Methods making use of common eutectic solders in novel ways are outlined in section 2.2.

Measurements of various thermophysical properties of solder alloys--both eutectic and noneutectic--are well underway (section 2.3). Values for the thermal conductivity and coefficient of expansion for some systems are given. Advances in the mechanical properties measurements are described.

Section 2.4 is devoted to the initial results of the computer stress analysis program. Analytical methods have been applied to a trilayer bond of Si to Mo using a gold solder layer. Effects produced by varying the expansion coefficient of both the solder and the substrate are discussed.

2.0 TECHNICAL DISCUSSION

2.1 DIFFUSION BONDING

In a previous report it has been pointed out that non-standard bonding techniques must be employed in heat sinking large area silicon devices. Due to the disparity in thermal coefficient of expansion between silicon and most heat sinking materials, small temperature excursions during bonding are desired. On the other hand, solders resistant to the hardening effects of thermal cycling (usually high temperature solders) must be used. The use of the so-called "diffusion bond" presented an attractive approach to the solution of this problem.

2.1.1 Solid-Liquid Interdiffusion Bond

Trilayer systems of Au-In, Au-Sn, and Au-(In+Sn) are electrodeposited by the procedures described in the Third Quarterly Report of this contract. These consisted of about 0.5 to 0.7 mil of Au deposited onto both the wafer and heat sink. A film of In and/or Sn 0.2 to 0.5 mil thick covered this and served as the "wet" layer during bonding. When both plates are coupled the In (Sn) wets and dissolves Au until a composition is reached where the melt cannot remain liquid. Precipitation of a high melting point solid begins and continues until the entire bonding layer has solidified. Further anneal then serves to homogenize the bond. It is believed that in this way one can obtain a hard, high melting point solder

while employing the moderate temperature excursions necessary to prevent high stresses in the wafers.

2.1.1.1 Results

Initial experiments were carried out with 2-inch diameter, 7-mil thick, p-type, silicon wafers on 1/8-inch thick molybdenum substrates. Several fair mechanical bonds were achieved with the indium "wet" layer but in every case wafers were found to have cracked severely. This is attributed to the thinness of the silicon and hence its inability to withstand the compressional forces imposed on it during cooling. In one case where the wafer did not crack, noticeable buckling occurred with the center of the wafer protruding about 10 mils above the substrate. Shortly thereafter a slight mechanical shock caused a crack to propagate across the wafer.

In more recent experiments wafers 20 mils thick have been used and the cracking problem has apparently been resolved. Many 2-inch wafers have been bonded (using both In and Sn) with good mechanical bonds to 1/8-and 1/32-inch moly plates. These include not only blank unprocessed silicon but several wafers containing more than 400 power transistors.

It should be noted that although the use of thicker wafers solves the problem of cracking, it presents the additional complication of a longer, high thermal resistance path for heat dissipation. Experiments to optimize wafer thickness so as to provide maximum heat dissipation with good mechanical strength will be in progress shortly. These experiments must also evaluate the need to provide a wafer in which diffused junction devices operate in a stress free environment (Phase III of program).

2.1.1.2 Voids in Solid-Liquid Diffusion Bonds

The major problem at this stage of the program is the presence of large voids in the solder layer. Examples of some voids which have been encountered are shown in Figures 1 and 2. These voids, in liquid-solid bonds are generally of two types, smooth-walled spherical voids randomly distributed (near the center of the wafer) and elongated irregular ones running parallel to the interface. In extreme cases voids encompassing up to 50 percent of the solder volume have been seen (Figure 2).

It is possible to enumerate a variety of causes for void formation in solid-liquid bonding:

(1) Trapped Gas--Since the electroplated layers of material are rough textured, small pockets of air are trapped between the wafer and substrate when they are placed in contact before the diffusion anneal. When the low melting point layer wets, this trapped gas becomes a bubble in the solder. These may appear as smooth-walled spherical holes along the initial bond interface and should be more prevalent near the center of the wafer where the chance of escape is very small.

(2) Outgassing--Because of the method used for making the metal layers, namely electrodeposition, a significant amount of gas and even possibly liquid may be included in the films. When the center layer wets out, these gases evolve (the liquids vaporize) and form voids similar to those of the trapped vapor but located within the "wet" material rather than along the initial interface.

(3) Nonuniform Cooling--It has been observed that the cooling process proceeds from the outer edges of the bonded wafer to the center. If the "wet" layer has not completely solidified upon

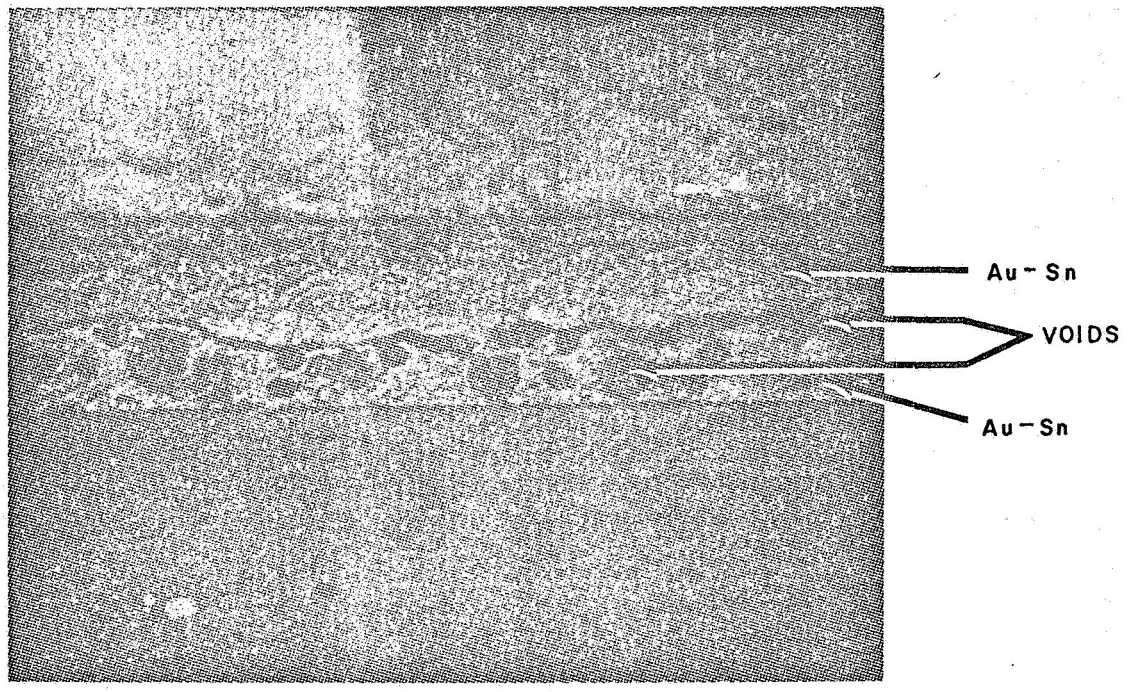

Figure 1. Smooth-Walled Voids in a Liquid-Solid Bond

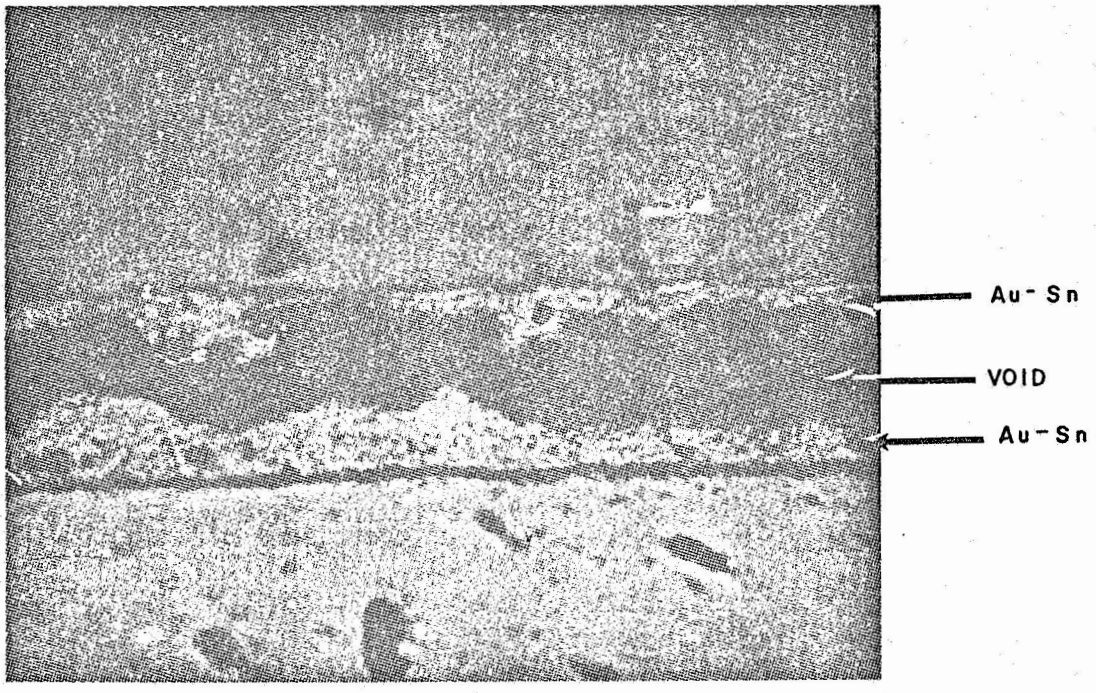

Figure 2. Large Voids in a Liquid-Solid Bond

removal from the annealing furnace, then the faster cooling at the edge "pins" it to the substrate. Further cooling causes the central region to bulge, due to the disparity in expansion coefficient, and "pillaring" of the unsolidified material in this region may occur. Alternate regions between connecting pillars appear as voids (Figure 3).

(4) Chemical Reaction--The presence of metallic oxides in the deposited layers may cause the release of gases when N_2 and H_2 are used as atmospheres for the anneal. Through the reactions

$$N + MO \rightarrow NO_2 + M$$
$$H + MO \rightarrow H_2O + M$$

steam and nitrous oxide may evolve and form the gas filled voids previously described.

(5) Dewetting--In systems where nonmating surfaces are put together (e.g. indium on the wafer and tin on the substrate) one surface may dewet leaving long wide voids along the initial interface.

(6) Diffusion Effects--If the diffusion anneal is continued after hardening, small voids may evolve due to the anisotropy in diffusion coefficient across an interface (Kirkendall effect). Other small voids may result from the clustering of vacancies and dislocations which are probably present in large numbers in electroplated films. Both of these effects are probably quite insignificant when compared with the others.

A solution to the void problem must be reached before satisfactory solid-liquid interdiffusion bonds are obtained. Experiments are to be started to determine feasible processes for

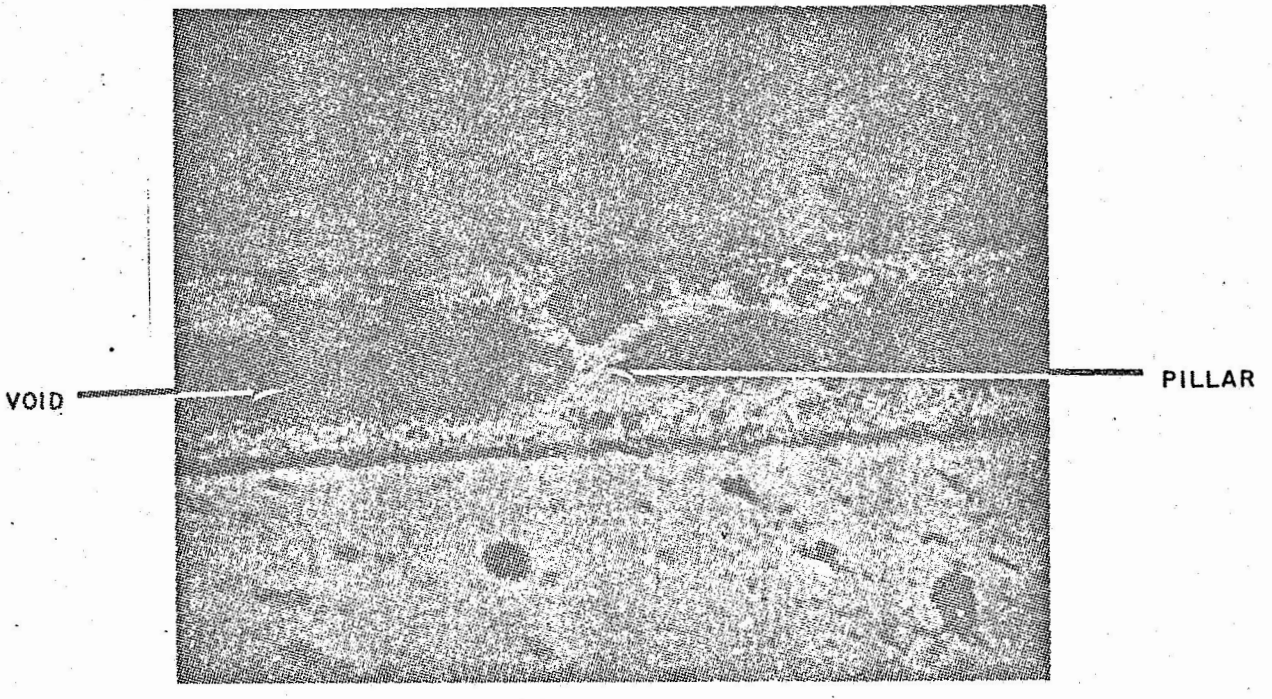

Figure 3. Pillaring in a Liquid-Solid Bond

eliminating voids. These will include vacuum anneal to control chemical reactions with protective atmospheres, and will also eliminate gases which would be surface trapped. "Prewetting" the central layer, under vacuum, to remove much dissolved gas so that it cannot evolve while bonding is going on. The use of binary and ternary alloys of Ga, Hg, In, and Sn which are liquid at room temperature will allow "scrubbing" and uniform wetting out of the furnace where it can be observed before anneal. Fluxes which have not previously been employed may be used before applying these liquids.

2.1.2 Solid State Diffusion Bonds

The binary diffusion couple has been used as an experimental tool for studying interpenetration of metals. Hetero-solid-solid bonds (Au-Ag; Au-Cu) where layered materials diffuse to form ideal solid solutions present an attractive alternative to liquid systems where undesirable intermetallics may be present. Although these bonds undoubtedly require longer anneals at higher temperatures than the SLID bonds, the advantages in both thermal and electrical conductivity might make this investigation worthwhile.

2.1.2.1 Results

During this report period diffusion bonds for several large (2-inch diameter) wafers have been made to molybdenum substrates using the Au-Ag diffusion couple at 300°C. These included a wafer of 400 power transistors which was bonded to a 1/32-inch moly plate. Tests of performance of the transistors indicated no deterioration due to bonding. Beta (the amplification factor) appeared to be unchanged and one could detect no series resistance (a possible indication of voiding) in the base-collector diode path.

These tests are, however, inconclusive since the devices which were bonded are not the best "strain gauges" and the series resistance test is not a sensitive one for voids. Bonds using wafers with MOS field effect transistors and diffused resistors (good strain gauges) should yield more significant information about strain propagation and voiding in all solid-state diffusion bonds.

Several silicon controlled rectifiers were bonded using the Au-Ag diffusion couple. These are composed of a silicon wafer sandwiched between two tungsten discs. Both the top and bottom surfaces of the wafer are plated with metals and the device is annealed for some 8-12 hours at 300°C.

Tests of the performance of these devices indicated a "forward voltage drop" comparable to the devices manufactured using other common solders. This forward drop may be used as a test for voiding. Some degradation in device performance indicated that surface plating, causing electrical leakage, was present.

Many wafer-wafer bonds have been made to investigate the homogeneity, and adherence characteristics of solid-solid bonds. These ranged in size from small chips to 2-inch wafers. In general these may be characterized as being of "good mechanical quality"; i.e. the wafers stick together well, but are beset with voiding problems somewhat similar to the solid-liquid bonds.

2.1.2.2 Voids in Solid-Solid Diffusion Bonds

Again, as in the case of the SLID bonds, the problem of major consequence, in making solid state diffusion bonds is voids. The characteristics of the voids obtained with solid-solid bonds are different than those when a liquid layer is present. For example,

even though outgassing of the solid layer occurs, there is no bubble formation with the probability of escape being much greater. The problems of Kirkendall effect, quenching and clustering and chemical reactions with N_2 and H_2 are probably minimal since in these bonds the anneal temperature is much lower than the solidus of either metal. There are, however, two major effects which may be responsible for the poor quality solid-state bonds.

(1) Surface Roughness--Electroplated gold and silver surfaces have a "matte" finish. This means that on a small scale there exist many hills and valleys rather than a smooth planar surface. When the contact area for bonding is small, moderate clamping forces produce pressures great enough to deform the gold and silver into one another and void-free bonding interfaces are observed. (This is the principle underlying the standard thermo-compression bond.) When a large area device is bonded (the same clamping system is used), the pressures at contact are greatly reduced, deformation does not occur and cross-section examination of the bonds reveal voids with irregular walls lying along the initial interface (Figure 4).

(2) Uneven Plating--In the plating systems used to date, the wafers were simply held in a flat-nosed alligator clip while immersed in the various plating baths. In this configuration the density of electric field lines--and hence the rate of metallic deposition--is greatest at the edge of the wafer. The result is a plate which is concave rather than planar. When such a surface is placed in contact with either a plane or another concave one, adherence can only occur at the highest points (i.e. the edges). This phenomenon has been observed with 1.5- and 2.5-inch diameter silicon wafer-wafer bonds that have been sectioned as a long cigar-shaped void running the entire length of the bond (Figures 5 and 6).

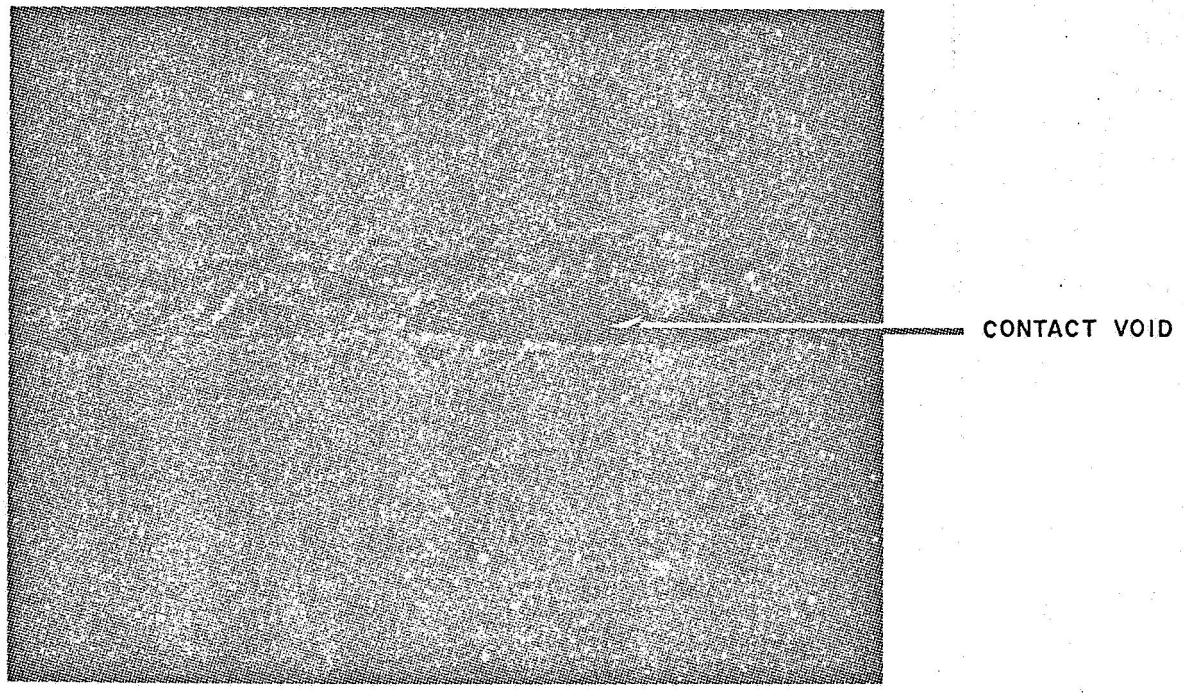

Figure 4. Voids due to Surface Roughness in Solid-Solid Diffusion Bonds

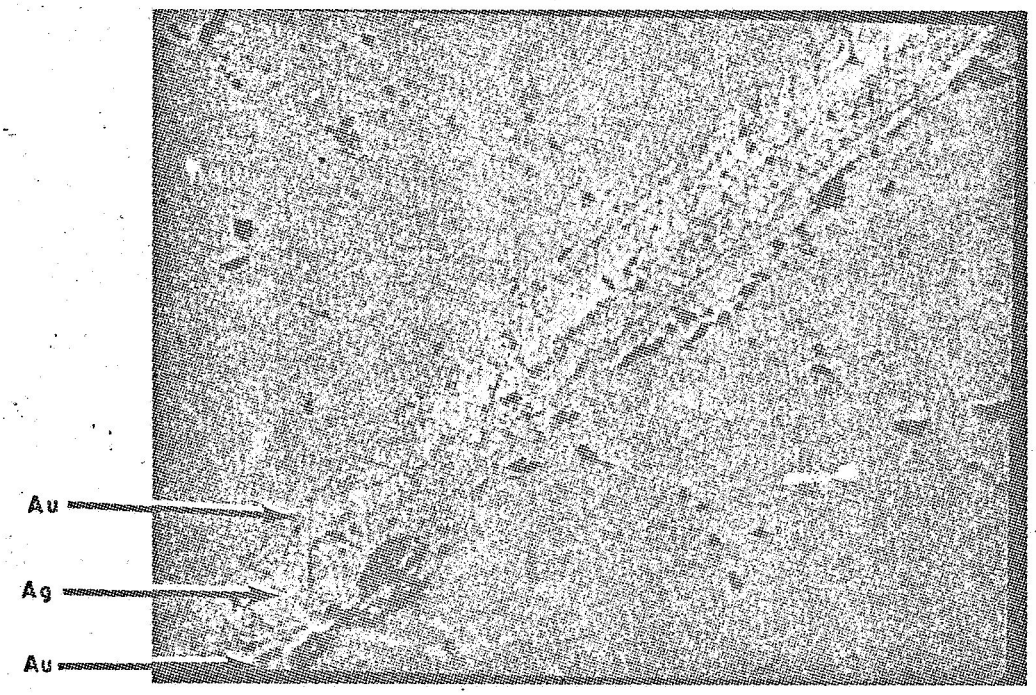

Figure 5. Complete Void Free Bond Near Edge of 1.5-inch Wafer (Au-Ag)

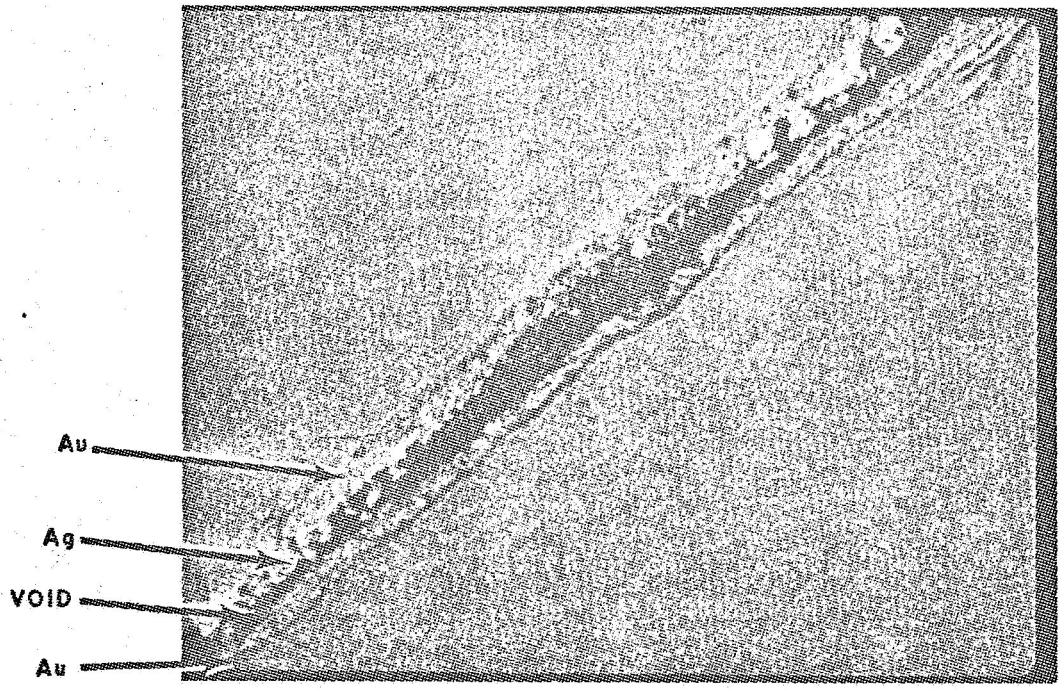

Figure 6. Voided Region Near Center of 1.5-inch Wafer Bond (Au-Ag)

Solutions to the surface roughness problem must be accomplished in some other way than by plating. The use of abrasion or other polishing techniques after plating on a thick layer of gold may help reduce both problems. A calculation of the pressure applied by the small needle of a thermocompression bonder should yield information on the feasibility of constructing clamps which could apply comparable loads to a 2-inch wafer. If such loading is possible, then the necessity of smoothing the surface will be removed.

To alleviate the concavity of the plated surface a "robbing" technique might be employed during plating. This involves placing the wafer to be electroplated in contact with a much larger metallic sheet. The electric field over the wafer is thereby caused to be uniform resulting in the deposition of a uniform thickness electroplate.

It is believed that when voiding problems are overcome and in cases where the longer, high temperature anneals can be tolerated, the solid-solid diffusion bond may provide a better bond than solid-liquid diffusion bonds which may form undesirable intermetallics.

2.2 EUTECTIC SOLDER METHODS

A complementary bonding study employing the commonly used eutectic solders (Pb-Sn, Au-Sn, Au-Ge, Au-Si) is in progress. For bonds where stresses are not important (e.g. studs to intermediate substrates) or where thick solder layers can be employed, these eutectic solders may have some usefulness.

Ideas for using these common solders currently point to shaped preforms which would provide a radially outward flow of metal after melt (e.g. star shaped). This would, in principle, have a sweeping effect and would provide a channel of escape for gases.

Another concept under evaluation is the use of solder in the form of very small spheres. For application, a monolayer of solder balls is held on the wafer by a sticky organic paste which evaporates at 100°C or so below the solder melting point. During anneal, therefore, the organic adhesive material burns off leaving a clean surface (it actually may act as a flux) well before the solder melts and wets the surface. It is noteworthy that the spherical shapes provide built-in channels for gas escape and voiding by trapping should be minimal. Preliminary results using the Au-Sn eutectic solder (217°C) indicate that excellent wetting of a gold-backed wafer can be achieved.

2.3 THERMOPHYSICAL PROPERTIES

2.3.1 Thermal Conductivity

The Colora Messtecknik thermal conductometer has been used to complete measurements of the thermal conductivity of various common eutectic solders. Five solders, Au-Sn (80-20), Au-Si (97-3), Au-Ge (88-12), Al-Si (89-11) and Pb-Sn (37-63) in the form of 0.65 x 1.0 inch pellets have been measured at 100°C. Three pellets of each solder have been measured a minimum of three times each and the results averaged. The results are presented in Table I.

TABLE I
MEASURED THERMAL CONDUCTIVITY
OF SELECTED EUTECTIC SOLDERS

Solder	Conductivity (Cal/cm/sec°C)
Au-Sn (80-20)	0.069
Au-Si (97-3)	0.031
Au-GE (88-12)	0.060
Al-Si (89-11)	0.196
Pb-Sn (37-63)	0.097

It is difficult to make comparisons to much of the existing data tables for thermal conductivity since in very few of them is the temperature of measurement quoted. This parameter is a decreasing function of temperature and hence we might expect our values (100°C) to deviate from any quoted in the room temperature range and be significantly lower than the values quoted at 4°K and lower. Figure 7 shows a plot of handbook values* for various Pb-Sn solders including a point for the alloy we have measured. Since no temperatures are given with the handbook data, a direct comparison may not be justified. However, a decrepancy appears to exist.

During this report period, several measurements in the Ag-In system have been made. These results are shown in Table II.

TABLE II
THERMAL CONDUCTIVITIES OF ALLOY SOLDERS
IN THE Ag-In SYSTEM

%In	Conductivity (cal/cm sec°C)
5	0.148
10	0.107
20	0.099

These values are significantly lower than that for pure silver (0.999 cal/cm sec°C) which may be due in part to voids in the samples left from casting. It would be expected, however, that the thermal conductance of the alloys should fall off sharply with increasing concentration at either end of the phase diagram.

* Metals Handbook, ASM, 1948 Ed., p. 26.

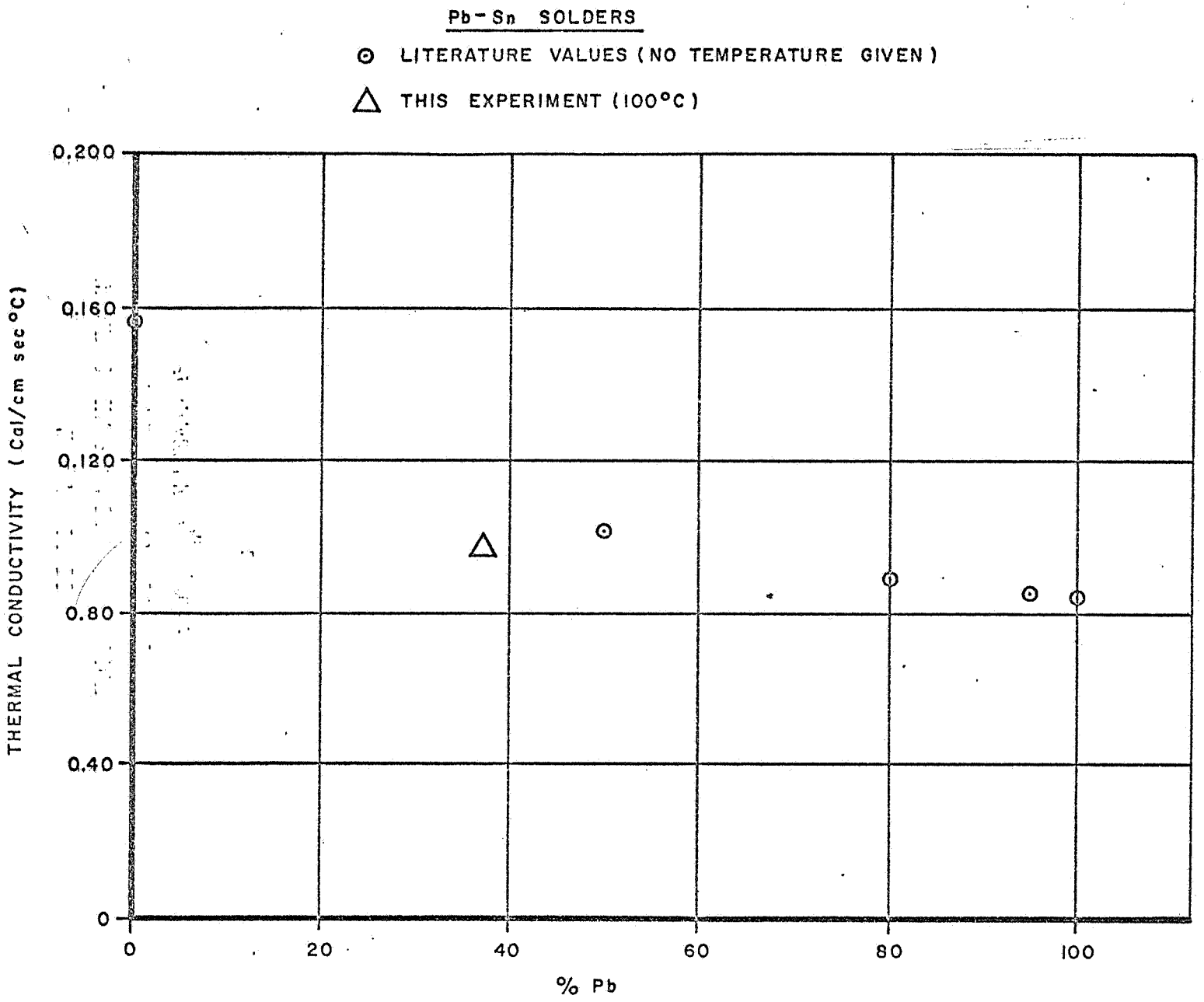

Figure 7. Thermal Conductivity of Common Pb-Sn Solders

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Recalibration of the apparatus using 99.999% pure metals of known conductivity is to be done in an effort to eliminate errors which may be present. It is believed that measurements with engineering accuracy are readily available and numbers can be obtained as quickly as samples are made.

2.3.2 Mechanical Properties

During this report period further instrumentation for making Young's Modulus and other related mechanical properties measurements was necessitated. Large amounts of deviation in the initial data for pure silver were attributed to the inherent elongation of the Instron testing machine rather than to the sample being pulled. To overcome this a strain gauge extensometer was used to measure sample elongation. This device clamps directly to the sample with knife edges set at a 2-inch gauge length. Elongations are monitored with a calibrated strain gauge and displayed on the y-scale of the Instron recorder. Some preliminary data has been obtained for the Young's modulus of pure silver and indications are that this parameter can now be measured to within a few percent.

Modifications in sample preparation techniques are necessary. The method now used (drawing molten metal into an evacuated tube) seems to yield short samples with voids in them. In the next period we will investigate the possibility of making fairly large diameter ingots and reducing these by drawing or swaging. This should not only reduce void densities and sizes but should aid in obtaining uniformity of composition.

2.3.3 Coefficient of Thermal Expansion

A quartz dilatometer has been used to make direct measurements of expansion coefficients of the solder materials. This is simply a dial guage mounted at the end of a quartz tube which holds

the sample. The tube is immersed in a suitable fluid (in this case silicone oil) which is heated causing the sample to expand. Coefficients are calculated from percentage expansions according to the equation

$$L(T) = L(T_o)\,[1 + \alpha\,(T-T_o)]$$

Original scheduling called for measurements of all the eutectic solders as well as the uncommon ones used in the bonding project. This may not be necessary as a fair amount of data may be obtained from the literature and spot checking may suffice. For example, an empirical equation has been published for the thermal expansion of the Ag-In system in the α solid solution (0-20% In) near room temperature. It is

$$\alpha_{Ag\text{-}In} = [18.73 + 0.02042\ (\%In) + 0.003576\,(\%In)^2] \times 10^{-6}$$

where 18.73 ppm/°C is the expansion coefficient of pure silver. A plot of this equation for the dilute region (<20% In) is shown in Figure 8. We have measured the coefficient for a 20 percent In solution and have obtained 20.2 ppm/°C which is within 3 percent of the quoted value.

Since the realm of binary metallic systems has been well investigated, we feel that a thorough literature search may make many measurements, especially in the dilute regions, unnecessary. This search has been initiated. Meanwhile some measurements at spaced intervals across the phase diagrams are continuing as planned.

2.4 STRESS ANALYSIS

The first results from the solution by superposition of the "stresses-in-joined-bodies" problem have been obtained. The method involves superposing four separate problems to yield a composite

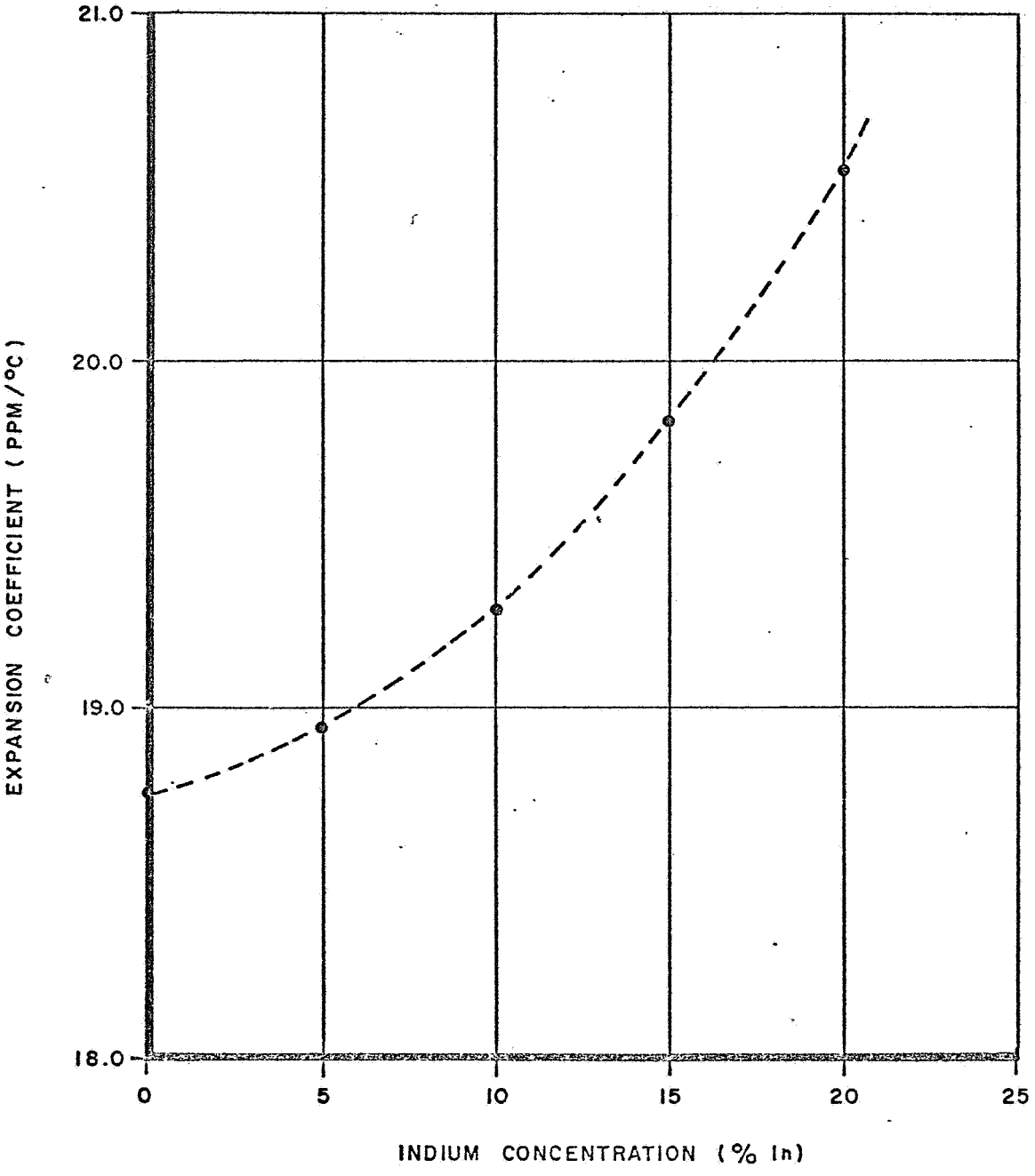

Figure 8. Thermal Coefficient of Expansion in Ag-In Solid Solution

cylinder with stress free surfaces. This approach was described in detail in the last report.

The task undertaken was the solution of a typical multilayer bond, namely Si, Au, and Mo. The silicon wafer--20 mils thick, 1 inch diameter--was assumed soldered by pure Au (2 mils) to a 1/8-inch thick molybdenum substrate. The thermal expansion coefficients for each layer are Si:3.3, Au:14.3 and Mo:5.5 in ppm/°C.

The applied stresses solved for in Solution III of the superposition give some preliminary indication of where the high stress regions are. It is apparent from the solution that the solder layer will be under very high tension stress--on the order of 30,000 psi, while the silicon is under a compressional stress of about half this amount. The moly substrate is the least stressed layer. Calculations varying the thickness of the gold layer have been done and these verify that the solder is somewhat "transparent" to the stress field. The molybdenum layer will be under tension up to solder thicknesses of 4 mils. If the molybdenum were only in contact with gold, it would be under compression. This indicates that the silicon's forces are transmitted through the Au to the molybdenum surface. A zero force is passed at solder thickness of 4 mils, implying a stress free molybdenum layer and for thicker gold layers the molybdenum and silicon have the same sign of stress.

No such zero points are reached for the silicon layer pointing out that a stress free wafer bond, using Au solder, is impossible. A calculation varying the wafer thickness indicates that to decrease the silicon stress by a factor of 2 one must more than double the wafer thickness. This may be prohibitive from a heat transfer standpoint.

Calculations varying the substrate (Mo) expansion coefficient confirm the expected in that increases in the coefficient cause the gold stresses to decrease (a better match) but further increase the silicon stresses. This latter effect also points out the solder "transparency" (Figure 9).

When the expansion coefficient of the solder layer is varied (Figure 10) the molybdenum and silicon are virtually unaffected as to applied force (Solution III). This implies that the solder has little to do with the determination of the equilibrium radius of the bonded system. It further indicates that with a 2-mil thick solder layer the silicon is primarily stressed by the molybdenum acting through the transparent solder.

The complete calculation at various expansion coefficients should further confirm this result.

These preliminary results seem to imply the necessity of a "matched" solder layer whose expansion coefficient lies somewhere between, Mo and Si. Calculations on the stress fields using such a layer are in progress and results should be forthcoming.

Initial results on the radial, Z, and hoop stresses in the Au layer do not indicate any dramatic differences from the hand calculated applied stresses. Toward the center of the wafer ($r < 0.3$ inch) all these are flat, become nonvariant with radius, and have values of about 30,000 psi.

3.0 CONCLUSIONS

The future of the diffusion bonding technique--both for SLID and SSID types--rests in the ability to eliminate the various voids which now plague the bonds. A concentrated effort to determine

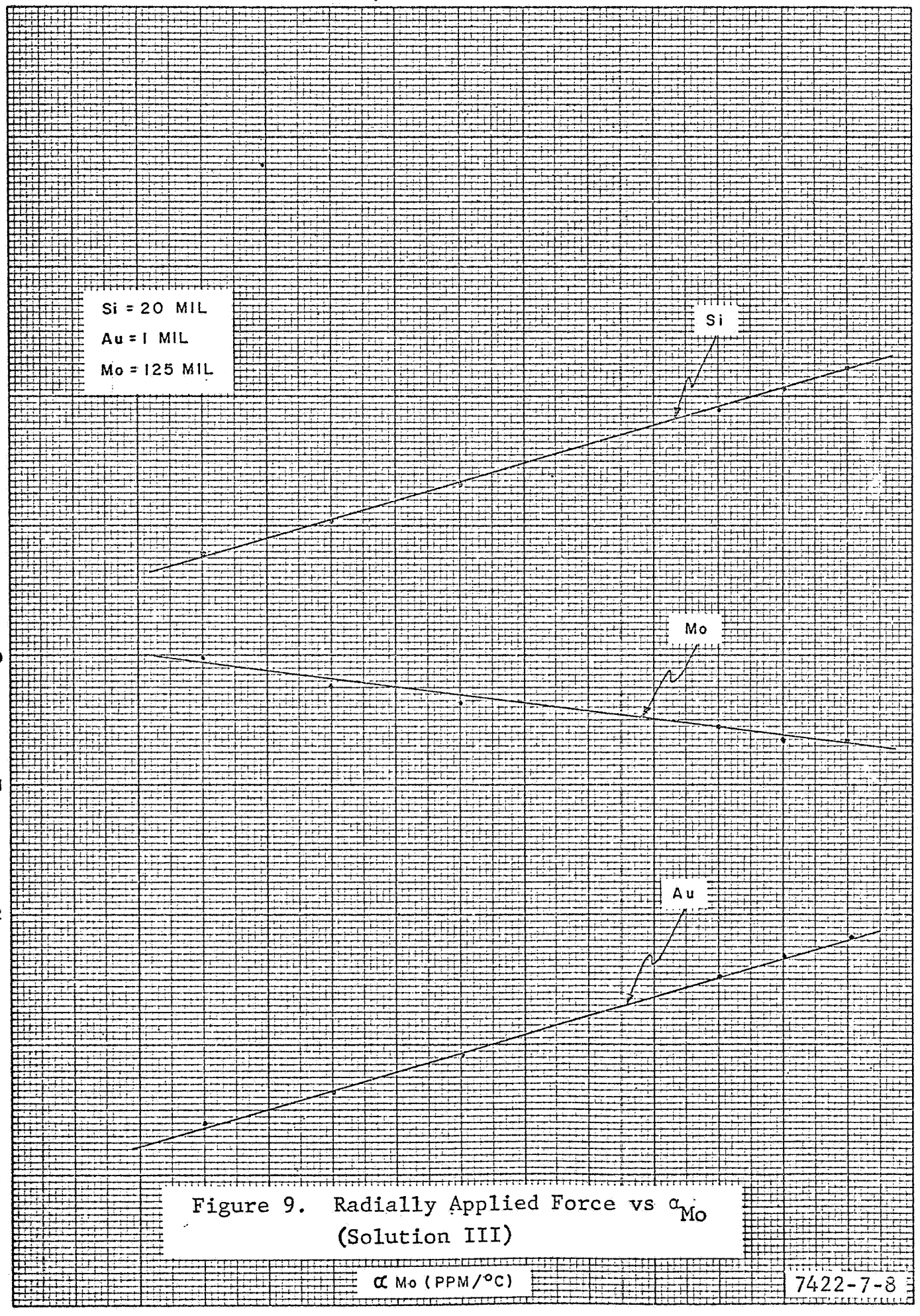

Figure 9. Radially Applied Force vs α_{Mo} (Solution III)

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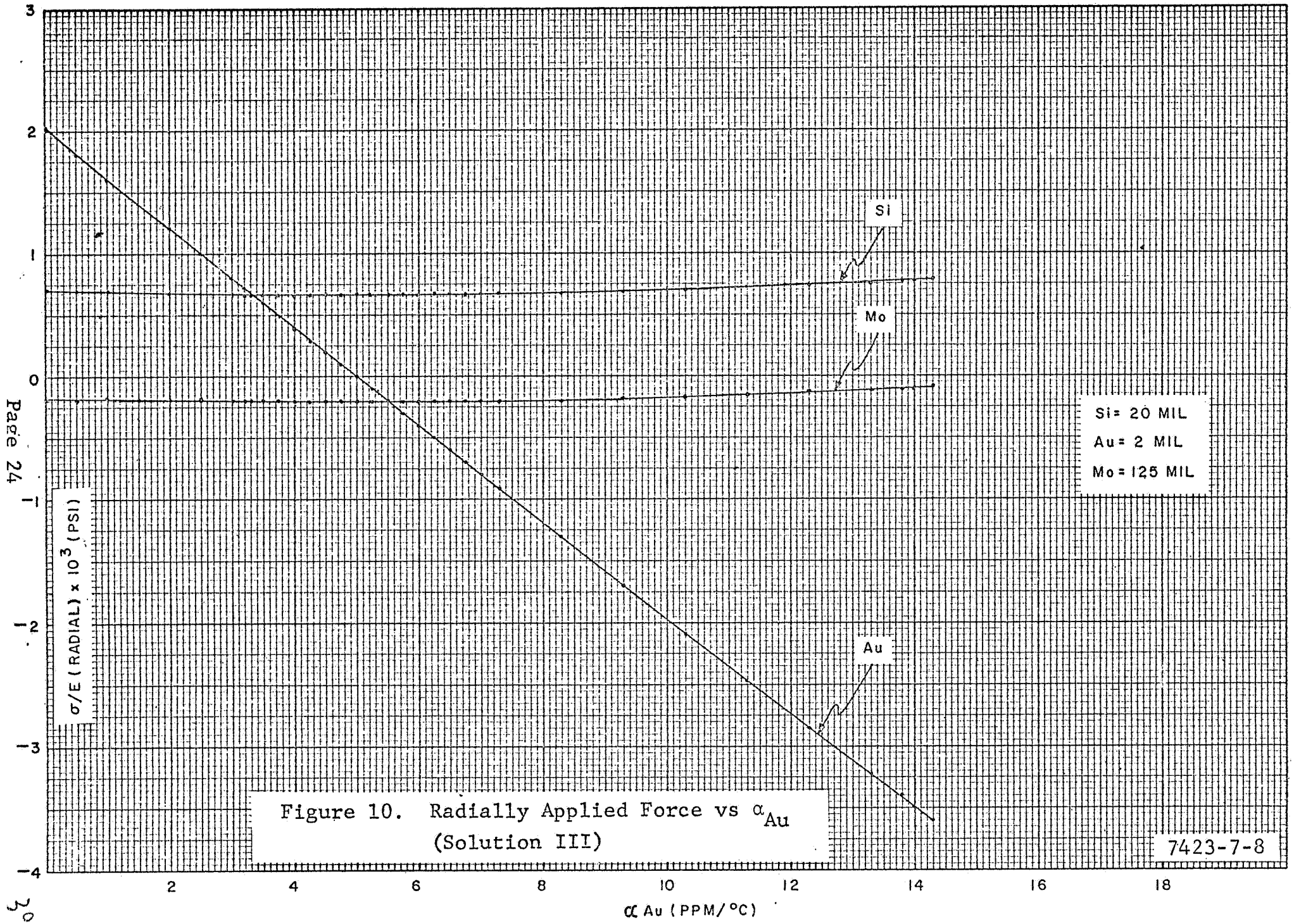

Figure 10. Radially Applied Force vs α_{Au}
(Solution III)

the character and causes of voiding should lead to the development of methods for their elimination. In most cases the problems are more of technique than an inherent defect in the bonding method. These problems have well known and frequently used solutions which are are to be modified to fit the particular needs of this project.

The mechanical strength of the 2-inch wafer bonds is to be further evaluated using thermal shock testing and repeated thermal cycling. Preliminary results (10 cycles from liquid nitrogen to hot plate) indicate good mechnical quality. The electrical and thermal conductivity characteristics, however, leave much to be desired. This is primarily due to the voids in the solder layer.

Attempts at bonding 2-inch wafers containing many power transistors have been successful using both SLID and SSID bonding procedures. These bonds are of good mechanical quality but, due to voiding, electrical and thermal quality is doubtful. Continued bonding and testing of these diffused devices in large wafers are planned for the next report period.

Measurements of the thermophysical properties of various alloy solders are continuing on a regular basis. Thermal conductivities for several solders have been measured. Although very reproducible, there has been some doubt about the absolute validity of these numbers due to shifting calibration and other difficulties with the thermal conductometer. Recalibration of the machine is in progress and modifications for use with the relatively high conductivity materials may have to be made.

Thermal expansion data has been obtained from the literature for the Ag-In solid solution and up to 20 percent indium. Measurements in this laboratory have confirmed some of these results. A further literature survey is expected to yield more significant data along these

lines. Determination of the thermal expansion of the eutectic solders is now being done. Results should be forthcoming.

The first results from the stress analysis computer program have been obtained. The results presented here are mostly hand calculated input data but they, in themselves, yield some insight into the stresses of the bonded system. Program results for a Si, Au, Mo bond are being evaluated. This data and information obtained in future runs will be interpreted and correlated in the next report period.

4.0 NEW TECHNOLOGY

No reportable items of new technology have been developed during this report period.